

EXPRESS MAIL LABEL NO. EV314044282US

DATED: 1 APRIL 2004

ATTORNEY DOCKET: MXIC 1571-1

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re Application of Inventors:
Chih Chieh Yeh et al.

Application No. _____

Filed: **1 April 2004 (herewith)**

Title: **Integrated Code and Data Flash
Memory**

Group Art Unit: unknown
Examiner: unknown

CUSTOMER NO. 22470

Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

INFORMATION DISCLOSURE STATEMENT UNDER 37 C.F.R. §1.56

Sir:

It is requested that the information identified in this statement be considered by the Examiner and made of record in the above-identified application. This statement is not intended to represent that a search has been made or that the information cited in the statement is, or is considered to be, material to patentability as defined in 37 C.F.R. 1.56.

Enclosed with this statement is a Form PTO-SB/08. The Examiner is requested to initial the form and return it to the undersigned in accordance with M.P.E.P. 609.

Also enclosed with this statement is a copy of each cited document as required by 37 C.F.R. 1.98. The exception to this, in accordance with the 05 August 2003 Official Gazette Notice in which the USPTO waives the requirement for submitting copies of U.S. Patent and Publications for cases filed after 30 June 2003, is that copies of U.S. Patent documents and copies of U.S. Patent publications are not being submitted.

If a written English-language translation of a non-English language document, or portion thereof, is within the possession, custody or control of, or is readily available to any individual designated in 1.56(c), a copy of the translation accompanies this statement, 37 C.F.R. 1.98(a)(3)(ii), and satisfies the requirement for a concise explanation of relevance, MPEP 609A(3).

This statement should be considered under 37 C.F.R. 1.97(b) because it is being filed within three months of the filing date of an application other than a continued prosecution application under 37 C.F.R. 1.53(d).

Fee Authorization. The Commissioner is hereby authorized to charge underpayment of any additional fees or credit any overpayment associated with this communication to Deposit Account No. 50-0869 (MXIC 1571-1). A copy of this authorization is enclosed.

Respectfully submitted,
HAYNES BEFFEL & WOLFELD LLP

Date: 31 March 2004

By: _____


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Substitute for form 1449A/PTO				Complete if Known	
INFORMATION DISCLOSURE STATEMENT BY APPLICANT <i>(use as many sheets as necessary)</i>				Application Number	1 April 2004 (herewith)
Sheet	1	of	3	First Named Inventor	Chih C. Yeh
				Group Art Unit	
				Examiner Name	
				Attorney Docket Number	MXIC 1571-1

U.S. PATENT DOCUMENTS					
Examiner Initials*	Cite No. ¹	U.S. Patent Document Number	Name of Patentee or Applicant of Cited Document	Date of Publication of Cited Document MM-DD-YYYY	Pages, Columns, Lines, Where Relevant Passages or Relevant Figures Appear
Kind Code ² (if known)					
A1	4,959,812		Momodomi et al.	09-25-1990	
A2	5,270,969		Iwahashi	12-14-1993	
A3	5,424,569		Prall	06-13-1995	
A4	5,448,517		Iwahashi	09-05-1995	
A5	5,515,324		Tanaka	05-07-1996	
A6	5,644,533		Lancaster et al.	07-01-1997	
A7	5,768,192		Eitan	06-16-1998	
A8	6,011,725		Eitan	01-04-2000	
A9	6,172,907		Jenne	01-09-2001	
A10	6,215,148		Eitan	04-10-2001	
A11	6,370,062		Choi	04-09-2002	
A12	6,436,768		Yang et al.	08-20-2002	
A13	6,458,642		Yeh et al.	10-01-2002	
A14	6,487,114		Jong et al.	11-26-2002	
A15	6,566,699		Eitan	05-20-2003	
A16	6,614,694		Yeh et al.	09-02-2003	
A17	6,643,181		Sofer et al.	11-04-2003	
A18	6,690,601		Yeh et al.	02-10-2004	
A19	Re. 35,838		Momodomi et al.	07-07-1998	
A20	2002/0179958		Kim	12-05-2002	

FOREIGN PATENT DOCUMENTS					
Examiner Initials*	Cite No. ¹	Foreign Patent Document		Name of Patentee or Applicant of Cited Document	Date of Publication of Cited Document MM-DD-YYYY
Office ³ Number ⁴ Kind Code ⁵ (if known)					
B1	JP	09162313A		Atsushi	06-20-1997
B2	JP	11233653A		Shigeki	08-27-1999
B3					
B4					
B5					
B6					
B7					
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B10					

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Sheet	2	of	3	Filing Date	1 April 2004 (herewith)
				First Named Inventor	Chih C. Yeh
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				Examiner Name	
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		Number	Kind Code ² (if known)			
A21	2003/0137873			Kawamura	07-24-2003	
A22	2003/0185055			Yeh et al.	10-02-2003	
A23						
A24						
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A26						
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FOREIGN PATENT DOCUMENTS								
Examiner Initials*	Cite No. ¹	Foreign Patent Document			Name of Patentee or Applicant of Cited Document	Date of Publication of Cited Document MM-DD-YYYY	Pages, Columns, Lines, Where Relevant Passages or Relevant Figures Appear	T6
		Office ³	Number ⁴	Kind Code ⁵ (if known)				
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INFORMATION DISCLOSURE STATEMENT BY APPLICANT				Application Number	1 April 2004 (herewith)
(use as many sheets as necessary)				First Named Inventor	Chih C. Yeh
Sheet	3	of	3	Group Art Unit	
				Examiner Name	
				Attorney Docket Number	MXIC 1571-1

OTHER PRIOR ART -- NON PATENT LITERATURE DOCUMENTS					
Examiner Initials*	Cite No. ¹	Include name of the author (in CAPITAL LETTERS), title of the article (when appropriate), title of the item (book, magazine, journal, serial, symposium, catalog, etc.), date, page(s), volume-issue number(s), publisher, city and/or country where published.			
	C1	BLOOM, ILAN, et al., "2-Bit Cell NV Memory Minimizes Chip Area with Less Masks," Nikkei Electronics Asia, January 2002, 11 pages			
	C2	DE BLAUWE, JAN, "Nanocrystal Nonvolatile Memory Devices," IEEE Transactions on Nanotechnology, Vol. 1, No. 1, March 2002, 72-77.			
	C3	HIROSE, M., "Challenges for Future Semiconductor Development," International Microprocess and Nanotechnology Conference, 6 November 2002, 47 pages.			
	C4	LEE, JAE-DUK, et al., "Effects of Floating-Gate Interference on NAND Flash Memory Cell Operation," IEEE Electron Device Letters, Vol. 23, No. 5, May 2002, 264-266.			
	C5	SHIN, YOOCHEOL, et al., "High Reliable SONOS-type NAND Flash Memory Cell with Al ₂ O ₃ for Top Oxide," Non-Volatile Semiconductor Memory Workshop, 2003, 2 pages.			
	C6	LEE, CHANGHYUN, et al., "A Novel Structure of SiO ₂ /SiN/High k Dielectrics, Al ₂ O ₃ for SONOS Type Flash Memory," Extended Abstracts of the 2002 International Conference on Solid State Devices and Materials, Nagoya, Japan, 2002, 162-163.			
	C7	YEH, C.C., et al., "PHINES: A Novel Low Power Program /Erase, Small Pitch, 2-Bit per Cell Flash Memory," IEEE IEDM, 2002, 931-934.			
	C8	PRINZ, E.J., et al., "An Embedded 90nm SONOS Flash EEPROM Utilizing Hot Electron Injection Programming and 2-Sided Hot Hole Injection Erase," NVM Workshop 2003, 2 pages.			
	C9	RUDEN, P. PAUL, et al., "Modeling of band-to-band tunneling transitions during drift in Monte Carlo transport simulations," J. Appl. Phys., Vol. 88, No. 3, 1 August 2000, 1488-1493.			
	C10	LEE, CHANG HYUN, et al., "A Novel SONOS Structure of SiO ₂ /SiN/Al ₂ O ₃ with TaN Metal Gate for Multi-Giga Bit Flash Memries," IEEE 2003, 4 pages.			
	C11	CHUNG, STEVE S., et al., "A Novel Leakage Current Separation Technique in a Direct Tunneling Regime Gate Oxide SONOS Memory Cell," IEEE 2003, 4 pages.			

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